

A LOW COST DC-DC Voltage Regulator Module (VRM) with Stepping Inductance for Fast Transient Response

Aslam Sher Khan*

Abdul Ahad Shaik**

B.JYOTHI***

PG Student, EEE Department,
Nimra College of Engg. & Tech.
Vijayawada, A.P, INDIA

Asso. professor & Head, EEE Dept.
Nimra College of Engg.&Tech.
Vijayawada, A.P, INDIA

Asso. Professor, EEE Dept.
Nimra College of Eng.&Tech.
Vijayawada, A.P, INDIA

Abstract - A single-phase fast transient converter topology with stepping inductance is proposed. The stepping inductance method is implemented by replacing the conventional inductor in a buck converter by two inductors connecting in series. One has large inductance and the other has small inductance. The inductor with small inductance will take over the output inductor during transient load change and speed up dynamic response. In steady state, the large inductance takes over and keeps a substantially small ripple current and minimizes root mean square loss. It is a low cost method applicable to converters with an output inductor. A hardware prototype of a 1.5-V dc-dc buck converter put under a 100-A transient load change has been experimented upon to demonstrate the merit of this approach. It also serves as a voltage regulator module and powers up a modern PC computer system.

Index Terms—Buck converter, fast transient, voltage regulator(VR).

I. Introduction

FAST transient response is a crucial issue in dc-dc converters for modern microprocessors. The load current may change between full load and nearly no load conditions within nano-seconds range. This fast load change demands the output terminal of the power supply to deliver full loading current within nano-seconds time range. Although a decoupling capacitor helps reduce the effect of the high current transient, the associated voltage regulator module (VRM) is still required to have a high slew rate of 150 A/ μ s or more.

The barrier of output current slew rate is determined by the equivalent output inductance of the buck regulator. Reducing output inductance is a way to satisfy the requirement. However, small inductance will produce side effects such as high

ripple current. Switching converter engineers are facing a new design challenge to provide high output current slew rate and maintain low ripple current, low ripple voltage, and high efficiency at the same time.

A small output inductance of a single converter may increase the output current slew rate, but this will also produce higher ripple voltage and ripple current which is not acceptable. Nevertheless, it is possible to reduce high ripple current by putting several converters in parallel and each converter has a relatively large output inductance.

An interleaving parallel converter is one special form of parallel converter configuration which produces small equivalent output inductance. An interleaved converter is generally accepted as a solution to provide fast transient response while keeping the output inductors from being too small. However, there are unresolved issues with the interleaved converter. It gives good performance during the transient state, but the steady state performance is still not satisfactory due to higher conduction losses induced by peak currents in each phase.

In addition to the many inductors in the multiple phases, the component count of associated circuits such as gate drivers and current sensing networks also multiplies with the number of phases put in parallel. Current sharing among the multiple phases of an interleaved parallel converter is also a challenging issue. Moreover, in order to produce wide bandwidth response to meet stringent requirement these days, high switching frequency is mandatory. Consequently, switching losses will also be increased.

A single-phase fast transient converter using stepping inductance is proposed in this paper. It is theoretically lossless, and is able to produce a high output current slew rate at the transient state and low ripple at steady state. It is an alternate solution to a multiphase power converter at low cost and it is easy to implement. The objective of this paper is to demonstrate this single-phase converter and the

capability to switch between different inductance values for transient and steady states. This paper also shows this single phase converter can be designed to meet tight VRM requirements such as the Intel VRD10.1.

II. BASIC IDEA

This section shows the basic configuration of the stepping inductance converter. Here only positive change of current is described.

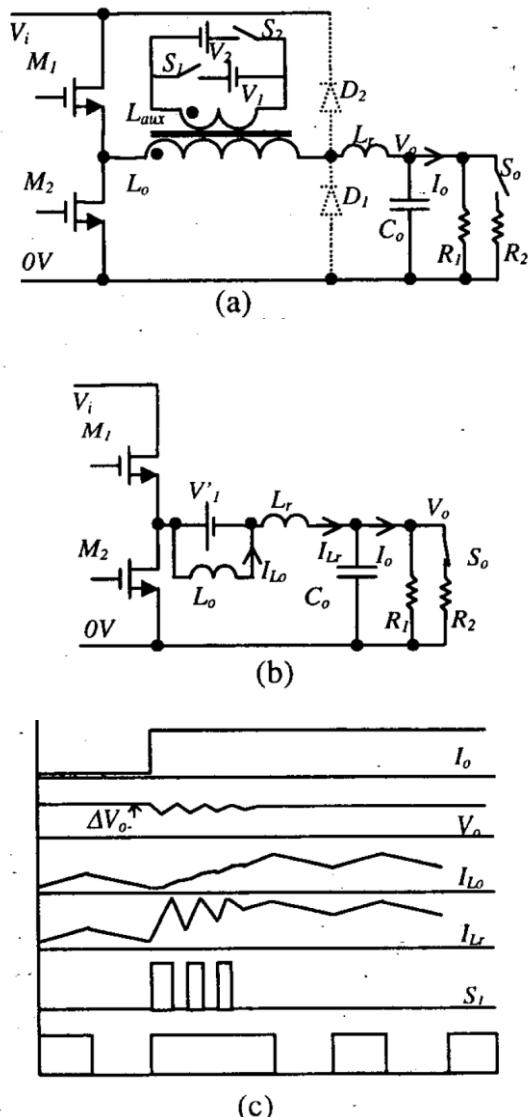


Fig. 1 Stepping inductance converter, a) Basic configuration b) Equivalent circuit during transient c) simplified operation

Fig. 1a shows the basic configuration of the stepping inductance converter switches M_1 , M_2 ,

output series inductors L_0 , L_r and output capacitor C_0 form and operate as a basic DC-DC buck converter. Inductor L_r is chosen to be much smaller than L_0 . Inductor L_{aux} is magnetically coupled with L_0 . L_{aux} , V_1 , V_2 , S_1 and S_2 form an auxiliary circuit to “short circuit” the large value inductor L_0 during load transient. S_1 is programmed to turn on during a fast and large increase in load current, S_2 is programmed to turn on during a fast and large decrease in load current. The number of turns of L_{aux} is chosen to reduce the reflected current flow through S_1 , S_2 in order to reduce their conduction losses.

Fig. 1b shows the equivalent circuit when S_1 is turned on under a step and large increase in load current. Once S_1 is turned on, the equivalent total output inductance will change from $L_0 + L_r$ to a much smaller L_r . This increases output inductor current slew rate in the period where transient occurred. This will result in much reduced voltage deviation due to large step change in load current.

Fig. 1c shows the operation of the fast transient converter by various waveforms. When the load current I_0 increase in a step, the output voltage starts to drop accordingly. The auxiliary switch S_1 with a series voltage source V_1 is programmed to turn on in order to provide a step reduction of the equivalent output inductance. The equivalent output inductance will change to a much smaller value L_r and provides a much higher slew rate output inductor current I_{Lr} . Once the fast output inductor current reaches the level of the output load current, the drop of the output voltage V_0 will stop and start to rise, as output inductor current is higher than the load current and flows into C_0 . Auxiliary switch S_1 can be programmed to turn off when the voltage V_0 rises back to a certain level.

As L_0 is much greater than L_r , the equivalent output inductor current will be dominated by I_{L0} after S_1 is turned off. Although magnitude of I_{L0} is increased during the period of S_1 is turned on, it is not high enough to reach to the level of load current I_0 , hence V_0 will drop again after S_1 is turned off. Nevertheless, S_1 can be programmed to turn on again when the output voltage drops below a certain level. These on and off states will repeat until the magnetizing current I_{L0} reaches a level equal to the load current. M_1 is expected to keep turning on between that on and off state of S_1 in order to ensure $I_{L0} = I_0$ as soon as possible and produce minimum transition time for the converter to go back to steady operation as quickly as possible.

The main purpose of the voltage source V_I is to optimized for minimum transition time. It keeps the output inductor's L_o current increasing when S_1 and M_1 are turned on. V_I can be chosen from 0V to a certain value such that the reflected voltage across L_o will not cause reverse current to flow through M_1 when S_1 is on. When the output current decreases in a fast a large step the operations are similar the mechanisms so described. At that time S_2 will turn on correspondingly and provide a high negative slew rate current to avoid voltage build up at C_0 . A transition period will be created in which S_2 will turn on and turn off until the current flowing in inductor L_o reduces to the load current.

III. IMPLEMENTATION

Practical circuit implement is simple. Voltage source V_I or V_2 can be realized by making use of the input voltage, although output voltage is also possible. Switches S_1, S_2 can be realized by small MOSFET L_r may the leakage inductance between winding L_o, L_{aux1} and L_{aux2} proper timing of S_1 and S_2 can be achieved by means of hysteresis control according to the change of output voltage V_o .

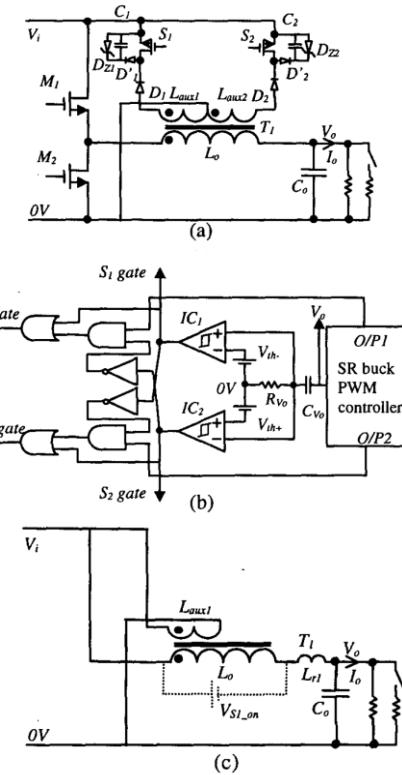
Fig. 2a shows the practical implement of the stepping inductance converter concept. Two separated windings or inductors L_{aux1}, L_{aux2} magnetically coupled to L_o and form a transformer T_I . S_1, S_2 are responsive to positive or negative change of load current. Diodes D_1, D_2 prevent reverse current flow. $D'_1, D'_2, C_1, C_2, D_{z1}, D_{z2}$ form a snubber circuit to absorb current reflected from leakage inductance L_{rl} when S_1 or S_2 is turned off. It is understood that other kind of snubber or non-dissipated snubber may also be used in this application.

Fig. 2b shows the control circuit. The SR buck PWM controller can be any typical PWM controller for Sync-Rect buck converter. Two hysteresis comparator IC_1, IC_2 , responsive for detecting the negative or positive change of output voltage. Logic circuit is added to ensure no simultaneous conduction of M_1 and M_2 , and no simultaneous turn on of switches S_1 and M_1 or S_2 and M_2 .

Fig. 2c shows a simplified equivalent circuit when S_1 and M_1 are turned on. S_1 is turned on if the output voltage drops below a predetermined level V_{th1} . M_1 will be turned on too as the SR buck PWM controller determine a voltage drop at output voltage V_o . After S_1 is turned on, the magnetizing inductor L_o is shorted out by an equivalent voltage source V_{S1-on} which has a value determined by the

input voltage and turn ratio of L_o and L_{aux1} . Hence the voltage across the equivalent leakage inductor L_{rl} becomes the difference of input voltage V_i , V_{S1-on} and V_o . It is designed to leave substantially large voltage across small leakage inductor L_{rl} to generate current with high slew rate and pumped to the output to counter act the output voltage drop. In practice, the overall equivalent inductance L_{rl} can be as small as the parasitic inductance of the PCB trace. Hence it is possible to tackle fast transient load in microprocessor application.

Fig. 2d shows simplified equivalent circuit when S_1 is turned off and M_1 is still turned on. S_1 is turned off if the change of output voltage has risen back to a predetermined level V_{th2} . V_{th2} is the trigger level of a hysteresis comparator which monitors the output voltage drop. The current I_{lr1} flowing in leakage inductor will be reflected to L_{aux1} and reset by the voltage source V_{Dz1} formed by snubber as described above. It is possible to use a lossless snubber to further reduce the losses in this reset mechanism. S_1 will keep turning on and off until the magnetizing current flowing in L_o rises up to the level of the load current.



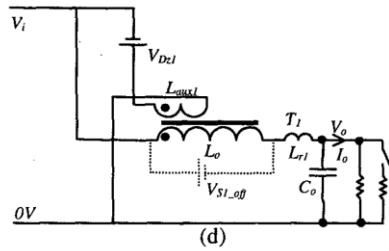


Fig. 2 Simplified practical implemental a) simplified circuit of stepping inductance converter b) hysteresis control and PWM circuit c) equivalent circuit when both S_1 and M_1 is turned on d) equivalent circuit when S_1 is turn off and M_1 is turn on.

IV. DESIGN PARAMETERS

Fig. 3 shows a microscopic and exaggerated view during loading transient condition.

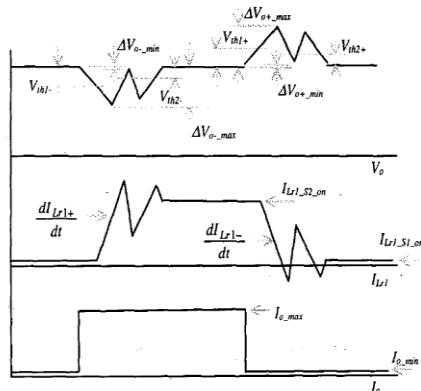


Fig. 3 Definition and exaggerated and microscopic' view between the relation of output voltage, inductor current and loading current.

Fig. 2c, Fig. 2d and Fig. 3 explain the transient. Here we assume a) the change of output voltage comparably small with the DC output voltage, b) the output loading current has a very large and stepping change, where the change of loading current is much larger than the ripple current flowing in L_{r1} . S_1 or S_2 will turn on when the output voltage drops or rises through the first threshold voltage V_{th1-} or V_{th1+} according to cases with a step increase or decrease in load current.

Positive output current slew rate dI_{Lr1+}/dt of L_{r1} depends on voltage across L_{r1} , and as

$$\frac{dI_{Lr1+}}{dt} = \frac{V_i - (V_o + V_i \frac{N_{Lo}}{N_{L_{aux1}}})}{L_{r1}}, \quad (1)$$

Similarly, negative output current slew rate dI_{Lr1-}/dt is

$$\frac{dI_{Lr1-}}{dt} = \frac{-(V_o - V_i \frac{N_{Lo}}{N_{L_{aux2}}})}{L_{r1}}, \quad (2)$$

where N_{Lo} = number of turn of L_o ,
 $N_{L_{aux1}}$ = number of turn of L_{aux1}

The behaviour of the output voltage transient can be analyzed according to the following mode by assuming a step change of loading current.

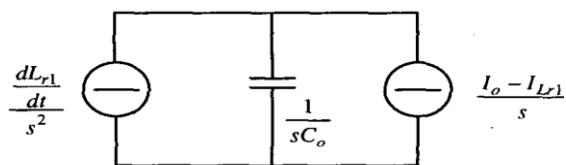


Fig. 4 Equivalent model during transient loading condition and S_1 or S_2 turn on

In order to find out the voltage change across C_0 , the turning point at which maximum deviated output voltage $\Delta V_{0-_{max}}$, $\Delta V_{0+_{max}}$ is produced has to be found out. The peaks can be found out by setting it's differentiation equal to zero. Physically, when current I_{Lr1} flowing in L_{r1} catches up with load current I_{o_max} or $I_{Lr1} = I_{o_max}$ output voltage will stop dropping and start to rise again. The maximum output voltage drop $\Delta V_{0-_{max}}$ can be worked out by simple circuit analysis and given by the following equation

$$\Delta V_{0-_{max}} = V_{th1-} + \frac{(I_{o_max} - I_{Lr1_S1_on})^2}{2C_o \frac{dI_{Lr1+}}{dt}}, \quad (3)$$

Similarly the maximum voltage rise $\Delta V_{0+_{max}}$ during Transient is

$$\Delta V_{0+_{max}} = V_{th1+} + \frac{(I_{o_min} - I_{Lr1_S2_on})^2}{-2C_o \frac{dI_{Lr1-}}{dt}}, \quad (4)$$

The inductor current will continue to increase or decrease until the changing output voltage hit a second threshold voltage V_{th2-} or V_{th2+} and S_1 or S_2 turn off. Nevertheless, excess output inductor current is formed when S_1 or S_2 turn off. This excess inductor current will keep the change output voltage in the same direction until the inductor current equal to loading current which forms a second turning. Beyond this second turning point the output voltage in change in the opposite manner. The negative minimum deviated voltage

V_{0_min} against V_o can be also found out by considering the voltage induced on C_o caused by the peak excessive inductor current I_{Lr1} dropping back to output loading current level, that is

$$\Delta V_{o_min} = V_{th2-} - \frac{3 \left[(I_{o_max} - I_{Lr1_S1_on})^2 + 2C_o \frac{dL_{r1+}}{dt} (V_{th1-} - V_{th2-}) \right]}{2C_o \left[(V_i + V_{Dz1}) \frac{N_{L0}}{N_{aux1}} + V_i \right] L_{r1}} \quad (5)$$

similarly positive minimum deviated voltage $V_{0+_{min}}$ again V_o is

$$\Delta V_{o+_{min}} = V_{th2+} - \frac{3 \left[(I_{o_max} - I_{Lr1_S2_on})^2 + 2C_o \frac{dL_{r1-}}{dt} (V_{th1+} - V_{th2+}) \right]}{2C_o \left[(V_i + V_{Dz1}) \frac{N_{L0}}{N_{aux2}} - V_o \right] L_{r1}} \quad (6)$$

An important criteria need to be drawn to avoid self oscillation of the hysteresis control mechanism. One must avoid the minimum deviated voltage V_{0_min} or $V_{0+_{min}}$ to cross over the output voltage level and touch the opposite threshold. The following criteria should be met at the sensing points,

$$V_{th1+} + V_{o-_{min}} > 0 \text{ and } V_{th1-} + V_{o+_{min}} > 0 \quad (7)$$

V. EXPERIMENTAL RESULT

A 5V input and output 2V 20A converter is built. Loading current is switched between $I_{o_max} = 20.5A$ and $I_{o_min}=0.5A$ at a frequency of 200Hz. The following figure shows the setup and values.

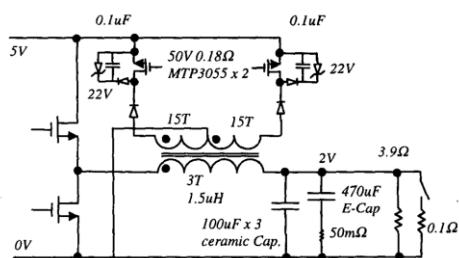


Fig. 5 simplified experimental circuit

Output inductor $L_0 = 1.5\mu H$, $N_{L0} = 3T$, with very small output ceramic capacitor of $C_o = 300\mu F$, and switching frequency $f_s = 300kHz$. Auxiliary winding $N_{aux1} = 15T$, $N_{aux2} = 15T$ are chosen 5 times of N_{L0} to reduce the losses of

auxiliary MOSFETs S_1 and S_2 . S_1 , S_2 are MTP3055 50V 0.18Ω small MOSFET. $DI = D2 = D'_1 = D'_2 = BYV27C$. Leakage inductance is measured as $L_{rl} = 100nH$. Which includes trace inductance $D_{z1} = 22V \frac{1}{2}W$ zener, $D_{z2} = 22V \frac{1}{2}W$ zener. $C_f=C2 = 0.1\mu F$. $V_{th+} = V_{th-} = 40mV$

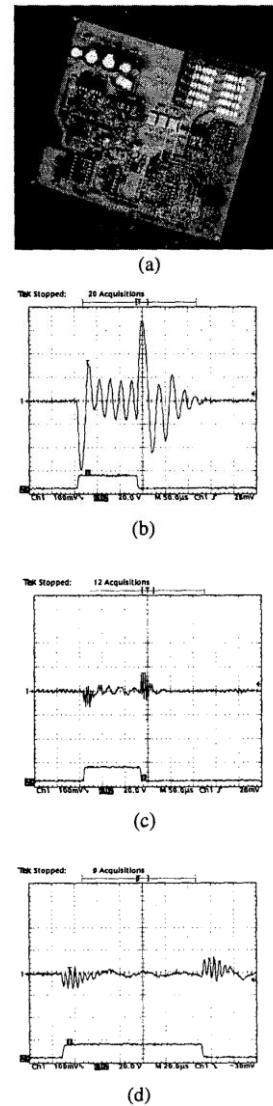


Fig. 6 Experimental result of output voltage variation, CH1- output voltage @ 100mV/Div, CH2 - load current signal , a) stepping inductance evaluation prototype b) without stepping inductance c) with stepping inductance d) with stepping inductance and extended time base.

The voltage deviations are calculated according to the equations so derived. Assuming

the ripple current of the output inductor is relatively small with compare to the loading current step change. Hence an approximation can be made,

$$I_{Lrl_S1_on} = I_{o_min} \text{ and } I_{Lrl_S2_on} = I_{o_max}$$

The maximum voltage change ΔV_{0_max} and ΔV_{0_+max} with 20A loading change is calculated as $\Delta V_{0_max} = 72mV$ and $\Delta V_{0_+max} = 103mV$. The experiment result show the real situation is better than the calculated result. The reason is investigated as 1) the auxiliary switch S_1 and S_2 actually turn on before the deviated output voltage hit the first threshold voltage V_{th1-} or V_{th1+} . It is caused by noise spikes induced from the very high slew rate of load current. 2) The loading current is not a real step changing loading current. Imagine a loading consist of switches and series resistor which has 0.1Ω and overall equivalent series inductance of $50nH$, it need to take $500ns$ to reach form $0.5A$ to $20.5A$. That $500ns$ is comparably large as the output inductor current need around $2us$ to increase $20A$, hence the output deviation is smaller than expected.

Results in Fig. 6b and Fig. 6c show almost 5 times reduction compared to unmodified buck converter. Fig. 6d shows a magnified view and it displays the small ripple voltage caused by the turn on and off of S_1 and S_2 . Conduction losses in auxiliary switch S_1 and S_2 are greatly reduced by the turn ratio of N_{L0} , N_{Laux1} and N_{Laux2} . The temperature rise of the MOSFETS S_1 , S_2 with $0.18\Omega R_{ds_on}$ and snubber zeners diodes D_{z1} , D_{z2} are below $5^\circ C$.

A transient fast change in input current will be introduced by the fast output current due to a fast load transient. This is true for all fast transient converters. An input filter is needed to slow down the input current during load transient condition. Such input filter can also provide filtering effect for steady state operation.

VI. CONCLUSIONS

A stepping inductor method for converters with an output inductor is presented. The stepping inductance converter is very suitable for low cost fast transient voltage regulator application. It can be applied to conventional buck converter to much improve transient response with only two additional small MOSFETs and diodes. It is also theoretically lossless.

Control circuit is also easy to implement and can be integrated with an existing buck PWM controller IC. Extra cost and design effort for such improvement is minimum, as only low cost small size component or logic circuit are needed.

Steady state performance is equivalent to today's sophisticated SR buck converter, and practically very little power loss-due to transient operation. Output ripple can be designed to be small as a large steady state output inductor can be used.

Input filter becomes not an extra cost as compare to interleaving converter as both need an input filter to suppress fast stepping input current during transient loading condition.

It is believed that such approach is very suitable for low cost fast transient response voltage regulator used on microprocessor and other fast loading change application.

VII. REFERENCE

- [1] F.C. Lee, "Voltage Regulator Module for Future Generation of Processors," *Tutorial Notes, Sixteenth VPEC Power electronics Seminar*, Virginia Tech., 1-1 15, September 1998
- [2] M.T. Zhang, M.M. Jovanovic and F.C.Y. Lee, "Analysis and Evaluation of Interleaving Techniques in Forward Converters," *IEEE Trans. Power Electron.*, Vol. 13, No. 4, pp. 690-8, 1998
- [3] C.K. Tse and N.K. Poon, "Nullor-Based Design of Compensators for Fast Transient Recovery of Switching Regulators," *IEEE Trans. Circ. & syst. Part I*, Vol. 42, No. 9, pp. 667-75, September 1995.
- [4] F.N.K. Poon, C.K. Tse, C.P. Iiu, "Very Fast Transient Voltage Regulator Based on Load Correction," *IEEE Power Electron Specialists Conference (PESC)*, Vol 1, pp. 66-71, June 1999
- [5] J. Wei, P. Xu, and F. C. Lee, "A high efficiency topology for 12 V VRM—push-pull buck and its integrated magnetic implementations," in *Proc. IEEE Appl. Power Electron. Conf. (APEC)*, 2002, pp. 679–685.